Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-3 (Canceled).

4. (Currently Amended) A method for synchronizing a digital video host system including a host computer **having a microprocessor,** a receiver circuit and a decoder circuit, the method comprising:

(a) coupling the receiver circuit with the decoder circuit only through separate nodes of a bus in the host computer;

(b) maintaining synchronization between the receiver circuit and the transmitter, without utilizing the host **microprocessor** ~~computer~~, by receiving a first transport packet from a transmitter with the receiver circuit; capturing a first system time clock (STC) timestamp at a start of receiving the first transport packet, the first STC timestamp being captured into a latch; obtaining a program clock reference (PCR) timestamp from the transport packet; comparing the first STC timestamp to the PCR timestamp to generate a comparison result; and adjusting an STC frequency based on the comparison result;

(c) capturing, with the decoder circuit, a system timestamp for an application system coupled with the decoder circuit but not with the receiver circuit; and

(d) adjusting the system timestamp with an offset based on a message delay time between the decoder circuit and the receiver circuit to maintain synchronization between the decoder circuit and the receiver circuit.

Claims 5-6 (Canceled).

7. (Previously presented) The method according to claim 4 further comprising:

(e) receiving data from the decoder circuit into a first register in a bus interface on the bus in the host computer;

(f) latching a second STC timestamp into a second register in the bus interface after receiving the data from the decoder circuit; and

(g) providing the second STC timestamp to the decoder circuit by way of the second register.

8. (Previously presented) The method according to claim 4 wherein the application system comprises an audio-visual system and the decoder circuit comprises an audio-visual interface.

9. (Previously presented) The method according to claim 4 wherein the application system comprises a networked computer system and the decoder circuit comprises a computer network interface.

Claims 10-12 (Canceled).

13. (Currently Amended) A system for synchronizing a digital video host system including a host computer **having a microprocessor**, a receiver circuit and a decoder circuit, the system comprising:

(a) a bus in the host computer having the receiver circuit and the decoder circuit on separate nodes thereof;

(b) the receiver circuit being adapted to maintain the synchronization between the receiver circuit and the transmitter without using the host **microprocessor**~~computer~~ and comprising: a parser adapted to obtain a program clock reference (PCR) timestamp from a first transport packet, the first transport packet including the PCR timestamp; a first latch coupled to the parser, the first latch being adapted to capture a first system time clock (STC) timestamp near a beginning of receipt of a first transport packet from a transmitter by the receiver circuit; a comparison device coupled to the parser and to the latch, the comparison device being configured to compare the STC timestamp to the PCR timestamp so as to generate a comparison result; and a first adjuster coupled to the comparison device, the first adjuster being adapted to adjust a frequency of the system time clock based on the comparison result;

(c) a second latch in the decoder circuit, the second latch being adapted to capture a system timestamp for an application system coupled with the decoder circuit but not with the receiver circuit; and

(d) a second adjuster coupled to the decoder circuit, the second adjuster being adapted to adjust the system timestamp with an offset based on a message delay time between the decoder circuit and the receiver circuit to maintain synchronization between the decoder circuit and the receiver circuit.

Claims 14-15 (Canceled).

16. (Previously presented) The system according to claim 13 further comprising:

(e) a first register in a bus interface comprised by the bus in the host computer, the first register being adapted to receive data from the decoder circuit; and

(f) a second register in the bus interface, the second register being adapted to latch a second STC timestamp after the first register receives the data from the decoder circuit,

wherein the second STC timestamp is provided to the decoder circuit by way of the second register.

17. (Previously presented) The system according to claim 13 wherein the application system comprises an audio-visual system and the decoder circuit comprises an audio-visual interface.

18. (Previously presented) The system according to claim 13 wherein the application system comprises a networked computer system and the decoder circuit comprises a computer network interface.

19. (Previously presented) The method according to claim 4 wherein the offset is scaled by a nonunity value.

20. (Currently amended) A method for synchronizing a digital video host system including a host computer **having a microprocessor**, a receiver circuit and a decoder circuit, the method comprising:

(a) coupling the receiver circuit with the decoder circuit only through a bus in the host computer

(b) maintaining synchronization between the receiver circuit and the transmitter, without utilizing the host **microprocessor** ~~**computer**~~, by receiving a first transport packet from a transmitter with the receiver circuit; capturing a first system time clock (STC) timestamp at a start of receiving the first transport packet, the first STC timestamp being captured into a latch; obtaining a program clock reference (PCR) timestamp from the transport packet; comparing the first STC timestamp to the PCR timestamp to generate a comparison result; and adjusting an STC frequency based on the comparison result;

(c) receiving data from the decoder circuit into a first register in a bus interface comprised by the bus;

(d) latching a second STC timestamp into a second register in the bus interface after receiving the data from the decoder circuit; and

(e) providing the second STC timestamp to the decoder circuit by way of the second register.

21. (Previously presented) The method according to claim 20 wherein the decoder circuit comprises an audio-visual interface.

22. (Previously presented) The method according to claim 20 wherein the decoder circuit comprises a computer network interface.

23. (Previously presented) The system according to claim 13 wherein the offset is scaled by a nonunity value.

24. (Currently amended) A system for synchronizing a digital video host system including a host computer **having a microprocessor**, a receiver circuit and a decoder circuit, the system comprising:

(a) a bus in the host computer that couples the receiver circuit with the decoder circuit;

(b) the receiver circuit being adapted to maintain the synchronization between the receiver circuit and the transmitter without using the host **microprocessor** ~~computer~~ and comprising: a parser adapted to obtain a program clock reference (PCR) timestamp from a first transport packet, the first transport packet including the PCR timestamp; a first latch coupled to the parser, the first latch being adapted to capture a first system time clock (STC) timestamp near a beginning of receipt of a first transport packet from a transmitter by the receiver circuit; a comparison device coupled to the parser and to the latch, the comparison device being configured to compare the STC timestamp to the PCR timestamp so as to generate a comparison result; and a first adjuster coupled to the comparison device, the first adjuster being adapted to adjust a frequency of the system time clock based on the comparison result;

(c) a first register in a bus interface comprised by the host-system bus, the first register being adapted to receive data from the decoder circuit; and

(d) a second register in the bus interface, the second register being adapted to latch a second STC timestamp after the first register receives the data from the decoder circuit, wherein the second STC timestamp is provided to the decoder circuit by way of the second register.

25. (Previously presented) The system according to claim 24 wherein the decoder circuit comprises an audio-visual interface.

26. (Previously presented) The system according to claim 24 wherein the decoder circuit comprises a computer network interface.